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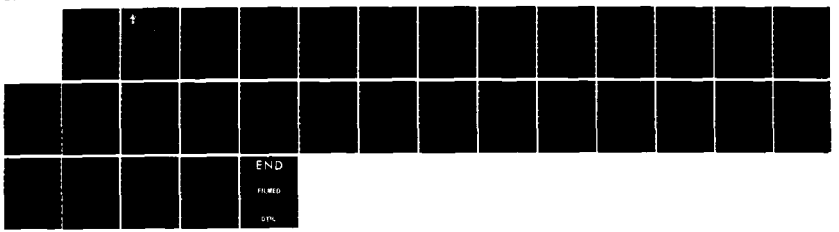

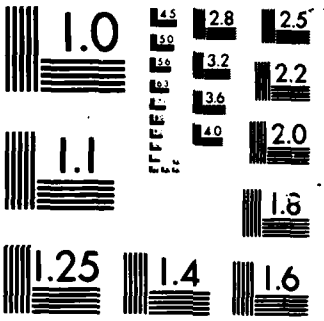

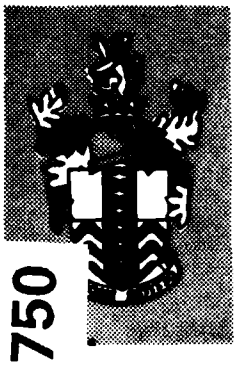

RSRE MEMORANDUM No. 3872

ROYAL SIGNALS & RADAR ESTABLISHMENT

THE DESIGN AND CONSTRUCTION OF A MODULE TO DEMONSTRATE A METHOD FOR TRANSMISSION OF DATA FROM A MEDICAL IMPLANT

Authors: I Morgan, J D Benjamin

PROCUREMENT EXECUTIVE,
MINISTRY OF DEFENCE,
RSRE MALVERN,
WORCS.

RSRE MEMORANDUM No. 3872

UNLIMITED

ROYAL SIGNALS AND RADAR ESTABLISHMENT

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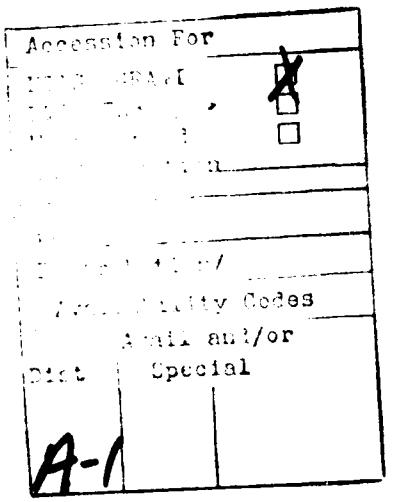
TITLE: THE DESIGN AND CONSTRUCTION OF A MODULE TO DEMONSTRATE A METHOD FOR TRANSMISSION OF DATA FROM A MEDICAL IMPLANT

AUTHORS: I Morgan and J D Benjamin

DATE: August 1985

SUMMARY

This report describes methods of powering devices to which only a/c contact can be made and receiving data transmitted back from them. Examples of such devices include medical implants which communicate with the external environment via ultrasound or rf links. Two breadboard systems have been built to demonstrate the techniques. In both the device is powered by picking up an ac input and rectifying it. A signal voltage detected by the device is encoded as a frequency, transmitted and decoded. In one case this is performed on a separate channel from that used to power the device. In the other only one channel is used for both signals, and data is transmitted by modulating the impedance presented by the device. The resulting modulation of the input signal was picked up by the external circuit and decoded.



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THE DESIGN AND CONSTRUCTION OF A MODULE TO DEMONSTRATE A METHOD FOR TRANSMISSION OF DATA FROM A MEDICAL IMPLANT

I Morgan and J D Benjamin

CONTENTS

FIGURES AND TABLES

1 INTRODUCTION

1.1 Objective

As technology has moved forward so the size of integrated circuits has decreased while the number of individual components contained in each IC has increased. This has occurred to such an extent that it is now possible to implant electronics into the human body. Examples of this include heart pacemakers and cochlea implants (1). The purpose of this project is to demonstrate a means of powering such devices externally and also of receiving data from the implant. Two such methods are shown, the first using two channels with one to input power to the device and the second to transmit the data; the second method uses just one channel to transmit both power and data. The data is in the form of a variable 0-1 V dc input and this is transmitted as a frequency to the external circuit where it is converted back to a voltage and output.

1.2 Design Procedure

There were two basic concepts around which to build a circuit, as shown in Figure 1. In the first, simpler, method it would prove necessary to utilise two separate ultrasonic transducers to provide the two channels. In practical situations this could cause problems of interference and alignment between them, and it was therefore agreed that the latter circuit would prove a better design. However the first circuit (Figure 1.1) was simpler to design and construct so it was built first, and the experience gained facilitated the subsequent construction of the second circuit (Figure 1.2).

A block diagram of the first design is shown in Figure 1.1. An ac power supply with a small output impedance was constructed. The ac signal was transmitted through a capacitive link rectified to power a voltage to frequency converter, the signal from which was passed through another capacitor before being converted back to a voltage using a frequency to voltage converter. Once this design was built and working, the circuit shown in Figure 1.2 was built. In this second case the incident signal not only powered the device but was also incident on a modulated load to produce amplitude modulation of the source voltage. This was decoded by the external circuitry. This necessitated the addition of the modulation and filter circuitry.

All the design was to be done on Breadboard with the completed circuit soldered to stripboard and placed in boxes for demonstration purposes.

2 DESIGN OF CIRCUIT ONE

2.1 Power Supply

The block diagram shown in Figure 1.1 consists of two separate parts; everything to the right of the three capacitors will now be known as the implant and everything to the left as external circuitry. The only way to get from the external circuit to the implant is through the capacitors. Since the impedance of a capacitor is inversely proportional to frequency, when frequency is zero, the impedance of a capacitor is infinite and all dc is blocked by it. Since it is intended to make the implant side as small as possible and also unhindered by any form of manual connection such as a wire, any power supply must be on the off-chip side and furthermore it needs to be ac in order to pass through the capacitors.

The original specification required that the supply must run at 1 MHz to enable simple filtering between it and the coded frequency in a subsequent circuit. There was no ac supply readily available to work at such frequencies, hence a signal generator which could produce such a high frequency, but very little current was used, and was amplified and its impedance reduced using the circuit shown in Figure 2. This gave an output impedance of only about 40 Ω. Both the 30 Ω resistor and the power transistor were heat sunk initially when the power supply was at a dc level of 30 V. But, it was found that this could be tuned down to 12 V with no noticeable difference in performance, and as a result 6 W resistors could be used with no heat sink on the transistor.

2.2 Capacitors

The capacitors, while very simple in themselves, lie at the heart of the problem. Their purpose is to represent the transmitting media between the implant and the external circuit and as such they block dc and only allow ac to pass. They therefore represent the imaginary separation between the implant and external circuits and also the physical boundary through which power has to go.

2.3 Rectification and Smoothing

The problem here lay in the 6 Volts peak to peak coming in while the voltage to frequency converter required a minimum of 8 V dc. A bridge rectifier seemed the obvious solution, however its output was not large enough, being only about 2 to 4 V depending on the type of diodes used. Putting three such bridges in series (see Figure 3) produced 12 V, but it proved incapable of producing the current required to drive the V/F converter.

Voltage multiplier methods were also tried, but these, being similar to bridge rectifiers, suffered from the same problems (see Figure 4). Clearly within each bridge there was a major source of impedance. The capacitors used had values of impedance not exceeding a few ohms at a frequency of 1 MHz and various tests on them with the diodes removed proved that they did not possess large impedances. Since the supply itself only had an impedance of 40 Ω, that too was not to blame for the large impedance. The cause therefore lay with the diodes. Several diode bridges were tested to find out which were the best at this frequency (see Table 1). The frequency was then altered to find the highest frequency at which the circuit could be operated. A major jump in the impedance occurred between 200 kHz and 300 kHz, as can be seen in Fig 5. Hence

the new operating frequency was tuned down to 200 kHz. In addition, two structures, each consisting of three bridge rectifiers in series, were placed in parallel as shown in Figure 6, thereby halving the impedance. Capacitors were placed on each input to isolate the dc level of one bridge from that of the next. Smoothing capacitors of the same value as the input capacitors were placed across the output of each individual bridge to remove any ripple on the output. This gave a very smooth final output which effectively did away with any need for a regulator.

2.4 Voltage to Frequency Converter

In order to be able to pass a dc voltage from the implant side to the external circuit, the voltage needs to be converted to an oscillating signal so that it may pass through the capacitors. To do this an RS 8415 Voltage to Frequency Converter was used which produces a square wave with a frequency proportional to the magnitude of the incoming voltage. The circuit as well as the integrated circuit to do this job is shown on RS data sheet 3021 as well as in Figure 7.

A single supply V to F converter was used and the resistance values set for a supply voltage of about 8 Volts dc. It was found that by altering R_2 the voltage at which a square wave was first produced could be altered. This was later to prove invaluable when selecting a zero point for the frequency to voltage converter, since its voltage range of 0-1 V had to be in a linear part of the graph shown in Figure 10. With this in mind a variable resistor was placed in series with R2 to enable a variation in the resistance to be easily made. C_{INT} and C_{REF} were chosen for the 100 kHz maximum frequency output.

There were two outputs from the V to F converter; f_o and $f_o/2$. Originally the f_o output was chosen but it had to be conditioned for the input to the F to V converter which had as one of its requirements the stipulation that the signal oscillated either side of zero volts. When fed through the output capacitor because the f_o output had considerably smaller troughs than peaks it failed to be 'averaged' by the capacitor and hence the peaks were only just above 0 volts. As a result, the $f_o/2$ output was chosen which had troughs and peaks of an equal length (see Figure 7). The gain adjust made very little difference and tended to be ignored.

2.5 FREQUENCY TO VOLTAGE CONVERTER

The frequency to voltage converter is the same integrated circuit as that used for voltage to frequency conversion. Its job is merely to reverse the process and convert a frequency into a dc voltage of proportional size. However, before this can be done the signal needs to be conditioned into the sort of signal that the F to V wishes to have. The prime consideration for this is a square wave which is less than the supply to the F to V, which is set at 15 V, and has a minimum value between 0 and -2 volts. However, before the signal can be adjusted to these dimensions it must first be set to a constant amplitude independent of the frequency. As the signal was passing through the capacitor (representing the ultrasonic transducer) it was attenuated, the amount of attenuation being inversely proportional to the frequency. As a result, different frequencies were altering the amplitude of the signal.

The first stage was to pass the signal through an op amp which was set to an infinite gain in order to cause the signal to clip at the rails, as shown in Figure 8. The signal produced was a square wave of amplitude equal to the supply rails of the op-amp and of frequency equal to that of the incoming signal. With infinite gain all of the signal at whatever frequency came out with the same amplitude. The next stage was to clamp the signal to the positive supply rail through a diode and a variable resistor. By taking an output off between the diode and the resistor and by altering the resistor value it was possible to 'clip' the negative part of the signal anywhere between 0 V and the negative supply. In this manner the signal's negative part was reduced in size to somewhere between zero and -2 volts. The signal was then fed into the F to V converter.

The F to V converter circuit was produced from the RS data sheet 3021 for a single supply F/V converter (see Figure 9), with one notable exception. The 1000 pF capacitor between the output at pin 12 and pin 3 was replaced by a 100 nF capacitor which made a far smoother output.

Adjustments were made to the various rheostats until the circuit was accurately calibrated and a graph produced showing the voltage fed in to the V to F against the voltage out from the F to V (see Figure 10) (also Table 2).

This concluded the design of the first circuit as shown in Fig 1.

3 DESIGN OF CIRCUIT TWO

3.1 Modulation

The most noticeable difference between circuit one and circuit two is that in circuit two the same capacitors are used to send the power through as are used to send the V to F signal back. This meant that some form of mixing or modulation had to be done. For this, frequency modulation or amplitude modulation immediately presented themselves. Both methods were tried.

3.1.1 Frequency Modulation

Frequency modulation is the modulation of the frequency or phase of the carrier wave. Depending on the frequencies of the modulated and the modulating signal, the mixed wave will look similar to that shown in Figure 11.1. There are several methods to frequency modulate two signals, most of which involve inductors and/or crystals, neither of which can easily be put on to integrated circuits. Since we are working on the on-chip side it becomes impossible to use either of these components. However there was one circuit that could be built, as shown in block diagram form in Figure 12. The circuit itself was complex and difficult to build.

Referring to Figure 12, the balanced modulator consisted of a diode bridge with the signal at one set of inputs and the carrier at another set. The 90° phase shift was provided by an RC network adjusted to give the correct shift and the adder was an op amp constructed in its adding mode. This produced a phase modulator which if integrated is frequency modulation. However the circuit failed to work effectively and was abandoned before too much time was wasted.

Other examined methods of frequency modulation included the use of an MC1496 integrated circuit, the diagram of which is shown in Figure 13. However this turned out to be more in keeping with amplitude modulation than frequency modulation.

3.1.2 Amplitude Modulation

Several methods were also tried for amplitude modulation, but these were simpler than frequency modulation methods and thus proved easier to construct and test. The first method involved feeding the V/F signal into a 2N2346 bipolar transistor through the base with the collector and emitter connected to the 200 kHz carrier signal. However the modulated signal produced at the emitter and collector was not properly amplitude modulated and appeared to be merely added together (see Figure 11.2). This does still have a component at the modulation frequency and could be used for data transmission but it has no sidebands or amplitude modulation.

The MC1496 integrated circuit was also tried, this time as an amplitude modulation, as shown in Figure 13. Unfortunately, it also appeared to only add the signals together. Hence the diode bridge circuit shown in Figure 14 was used. This modulated the signal to an extent that it appeared similar to that shown in Figure 11.3. The diodes used to do this were the OA47 as used in the rectification, but ordinary signal diodes would have done the job equally well. The modulated signal was passed back through the capacitors to the off-chip circuit where it could be demodulated.

3.2 Demodulation

The actual amplitude modulation was very small and recovering the original signal would not be easy without amplification. The circuit used for demodulation is shown in Figure 15. The modulated signal was taken off across the 30 Ω resistor of the power supply and passed through a 355 op amp set to a gain of one. This avoided altering the impedance between the power supply outputs and meant the signal came through the op amp unchanged. A 355 op amp was used because it had a slew rate that was capable of handling 200 kHz whereas the 741 used in circuit one was not fast enough.

Demodulation should have been a simple diode and capacitor in series, with an output taken off between them, the theory being that the diode half-wave rectifies the signal and the capacitor smooths out the 200 kHz leaving the original signal produced from the V to F. However, several diode and capacitor units were needed to remove most, if not quite all of the 200 kHz powering signal, leaving a very small V/F signal of about 60 mVpp. This V/F signal was reduced still further by increasing the frequency since it caused the impedance of the 15 nF capacitors (see Figure 18) to reduce enabling more of the signal to leak to ground. Once more, OA47 diodes were used as these produced the best output, but again faster diodes might well be better.

From here the small signal had to be amplified, once again using a 355 op amp. This time the gain was set to an infinite level so that the signal at the input clipped at the op amp's supply rails. This produced a square wave of amplitude between +12 V and -12 V at the frequency produced by the V to F converter. A separate supply was used to power the external circuitry of +15 V,

0 V, -15 V, because the dc supply into the power transistor had a large amount of ripple on it caused by its association with the signal generator. This ripple tended to find its way on to the input to the op amp and swamp the small signal from the V to F converter. Clamping the signal to the positive supply rail through a reverse biassed diode and a res'stor was done as before to produce the correct signal amplitude into the frequency to voltage converter. The resistor was adjusted until the signal amplitude lay between +12 V and -2 V.

The amplified signal was then fed into the frequency to voltage converter, to be converted back to the original dc voltage.

An amplitude modulated signal with a carrier frequency of w and a modulation frequency of m has frequency components at $w \pm m$. By filtering out one of these components and mixing with a signal of frequency w and filtering again, the modulation frequency m could be extracted. This should have the advantage over straight amplitude modulation detection that if a number of implants are all sending back a modulated signal, that the distribution of modulated signals can easily be identified.

An attempt was made to build such a circuit, using MF10 filter chips obtained from Radio Spares. The circuits were rather complex, separate clocks had to be provided for the chips, and difficulties were encountered in getting the circuits to work for signals of the size being returned, and this approach was abandoned through lack of time.

3.3 Calibration

The whole of circuit two contains four variable resistors which may be altered to calibrate the circuit. They are:-

3.3.1 Gain Adjust

This alters the frequency very finely from the voltage to frequency converter. It can be used in conjunction with R2 as a fine timer.

3.3.2 R2 - The 0 V Frequency Level Adjust

As can be seen from Figure 10 the plot of V_{OUT} against V_{IN} is only linear along a certain length. The job of R2 is to alter the frequency representing an input of 0 V into the V to F converter. This causes the range of 0-1 V into the V to F to be within frequencies that lie on the linear part of the graph in Figure 10. These frequencies are given in Table 2, and hence by selecting a linear part of the graph the equivalent frequencies can be found from Table 2 and a 0 V frequency selected to be set by R2. Accurate setting can then be done using the gain adjust mentioned above.

3.3.3 Offset Adjust

This variable resistor sets the zero level on the output of the frequency to voltage converter. By altering it any point between 1 V and the supply can be set as a zero at the output. The best results were

obtained when the offset adjust was set to a point just above the minimum voltage level.

3.3.4 The Clamp Resistor

As described earlier this resistor is connected between the +15 V supply rail and the input signal, through a reverse biassed diode, to the frequency to voltage converter. Its purpose is to alter the negative amplitude of the signal, and by altering its values the signal can be conditioned to the correct amplitude for input into the F to V converter.

4 THE DISPLAY MODULE

4.1 Construction

The circuit, which until this stage had been built on breadboard, was constructed on three different sheets of copper clad stripboard in order to go in three different boxes, as shown in Figure 16. Each box represented a specific part of the circuit. In the first box there was the external circuitry including the power supply, the demodulation and amplifiers and the frequency to voltage converter. Box two contained the capacitors representing the ultrasonic transducers and link. Within box three were stored the implant components comprising the bridge rectifiers, the voltage to frequency converter and the modulating circuit. The boxes were linked by a series of 2 mm connectors and 5 amp cable, colour coded to represent polarities.

4.2 Final Calibration

When final construction was completed final calibration could take place using the four variable resistors. Firstly a 0 V frequency was worked out from the graph in Figure 10 and Table 2 to give a linear relationship between the input voltage and the output voltage. R2 and the gain adjust were altered to provide such a frequency. Next the clamp resistor was altered to bring the signal into a range suitable to be fed into a frequency to voltage converter. Finally the offset adjust was altered to give the lowest 0 V reading but also a large range of movement as the input voltage was increased. A graph of V_{IN} against V_{OUT} in the range 0-1 V is shown in Figure 17. The gradient of the graph is 0.977; in fact it should be one!

5 DISCUSSION

There was only one major problem encountered in this project and that was producing the power required to drive the on-chip circuitry. A CMOS voltage to frequency converter IC was used which has a very small power consumption when it is not switching. However in its switching mode the power consumption greatly increases and this proved to be a problem. Adding to this difficulty was the frequency of the power supply which initially was 1 MHz. While the impedance of the capacitors fell away rapidly at higher frequencies, unfortunately so did the voltage produced from the diode bridges. Furthermore their impedance increased and the result was that any voltage produced fell away to zero, or close to that, when loaded by the implant circuitry. Considerable effort was expended in trying different diodes, different capacitors and different circuits to produce

the required output of around 8 volts dc. Eventually tests at different frequency levels were made and 200 kHz was identified as the highest frequency capable of powering the implant circuitry.

As for the demodulation and filtering the only problem appeared to be a gradual attenuation of the signal with increasing frequency as the 15 nF smoothing capacitors become less resistive to the signal. A stage is reached whereby the signal is so small at the input to the amplifier that the output signal becomes lost in noise. This caused a 'shake' on the dc level output of the frequency to voltage converter and at higher frequencies caused it to reduce to zero. It was notable that this effect was far worse, occurring at a much lower input voltage, when the circuit was first switched on. After about ten minutes the 'shake' only occurred outside the operating range and as such tended to be ignored.

Particularly if the circuit were integrated into ICs it would seem better to use faster diodes, such as Schottky diodes. The research so far completed would seem to indicate that faster diodes have lower impedances at the frequencies dealt with. Should the attenuator of the signal by the demodulation stage ever become a major problem, faster diodes are possibly one way to avoid this. Another way is to use smaller capacitors than the 15 nF ones currently being employed. This would increase the impedance of the capacitive link to ground and enable higher frequencies to be used, possibly up to an equivalent of 4 V, the maximum output of the frequency to voltage converter. The frequency to voltage converter must receive a signal at the input of frequency between 10 Hz and 100 kHz to function. This, apart from amplitude, is the only condition and it is this which provides the limit for the maximum output voltage.

6 CONCLUSIONS

The experiment was a success in that it achieved its aim of producing a dc signal from a dc input through a capacitive link. Since it needed only one channel, circuit two was a better design and should prove useful in future work on electronic implants in the human body. If a sensor producing an input voltage of 0-1 V is incorporated in the implant, signal frequencies well in excess of 20 Hz could be handled by the frequency encoded link. This is adequate for most applications.

7 ACKNOWLEDGEMENTS

The authors would like to thank Mike Uren for his advice and help and also fellow room residents Tim Fry and Phil Stone for useful discussions.

REFERENCES

1 A Custom LSI CMOS Chip for a Cochlea Implant, by H McDermott, Journal of Electrical and Electronics Engineering, Australia, Vol 4, No 4.

TYPE	DESCRIPTION	VOLTAGE PRODUCED	IMPEDANCE
SKB2/02L5A	In Line 1.6 A Package	2 V	-
KBL02	In Line 3 A Package	2 V	-
CV7845	Power Diode	2 V	-
CV7114	Signal Diode	3 V	500 kΩ
OA47	Gold Bonded Germanium Signal Diode	4 V	1 kΩ
7047	Signal Diode	4 V	1 kΩ

No high speed diodes were available for testing.
Schottky barrier rectifiers were too expensive to test.
Both might have offered better performance at 1 MHz.

TABLE 1

VOLTAGE IN (V)	VOLTAGE OUT (V)	FREQUENCY (Hz)
0.1	0.80	0
0.2	0.76	555.56
0.3	0.80	1086.96
0.4	0.88	1639.34
0.5	1.04	2127.66
0.6	1.06	2631.58
0.7	1.20	3225.81
0.8	1.26	3846.15
0.9	1.36	4444.44
1.0	1.42	5000.00
1.1	1.50	5555.56
1.2	1.58	6060.61
1.3	1.66	6666.67
1.4	1.72	7142.86
1.5	1.85	7407.41
1.6	2.00	8000.00
1.7	2.05	8333.33
1.8	2.15	9090.91
2.0	2.30	10000.00
2.25	2.54	11623.41
2.5	2.8	13157.89

TABLE 2

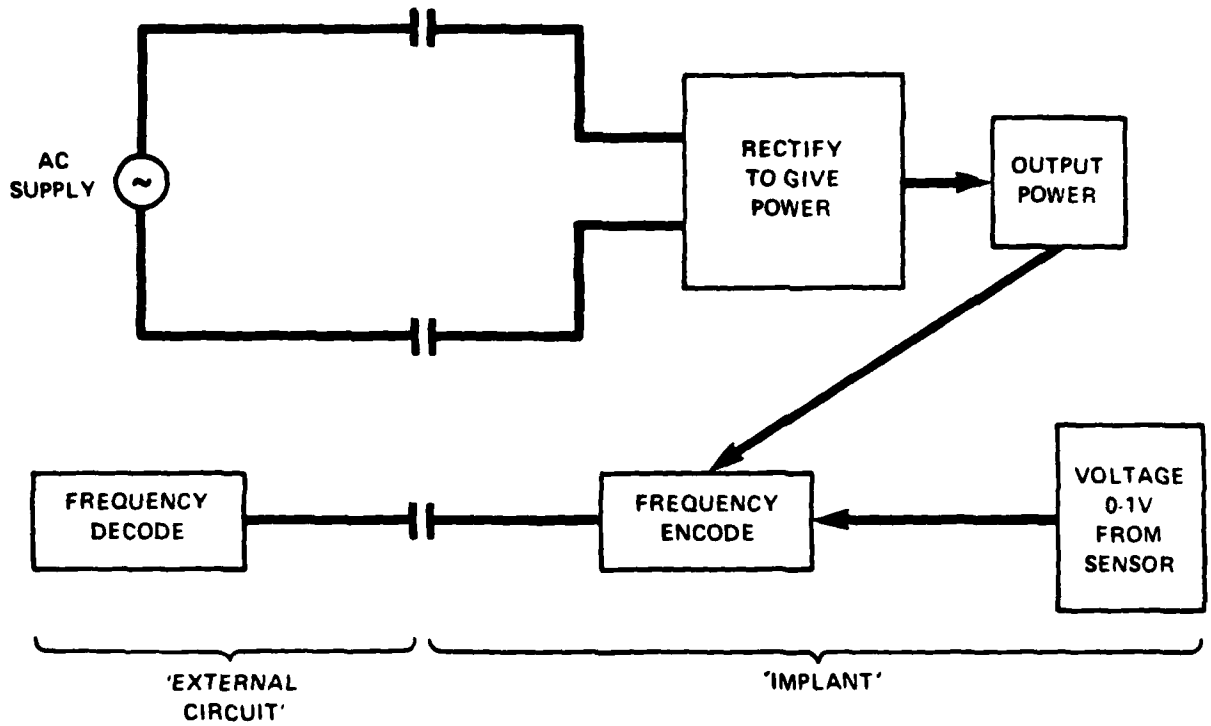

AC
SUPPLY
RECTIFY
TO GIVE
POWER
OUTPUT
POWER
FREQUENCY
DECODE
FREQUENCY
ENCODE
VOLTAGE
0-1V
FROM
SENSOR
'EXTERNAL
CIRCUIT'
'IMPLANT'

FIG 1.1

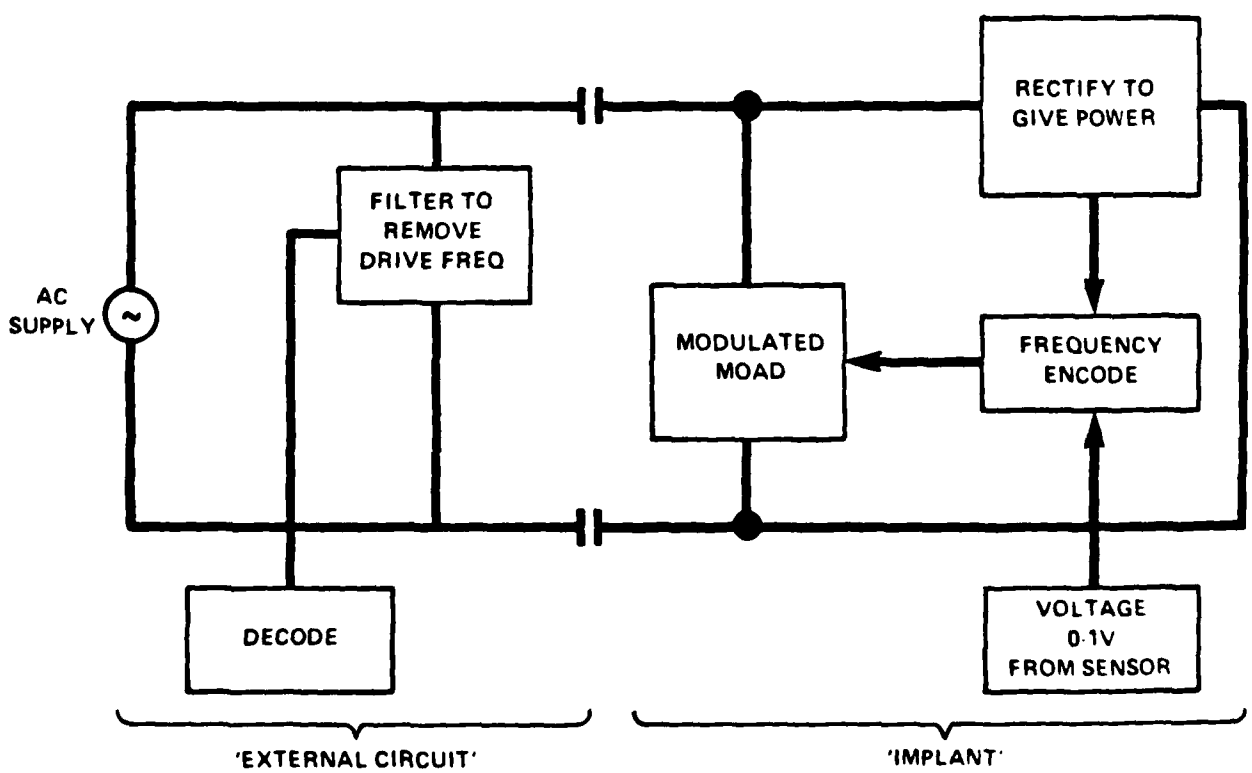

RECTIFY TO
GIVE POWER
FILTER TO
REMOVE
DRIVE FREQ
AC
SUPPLY
MODULATED
MOAD
FREQUENCY
ENCODE
DECODE
VOLTAGE
0-1V
FROM SENSOR
'EXTERNAL CIRCUIT'
'IMPLANT'

FIG 1.2

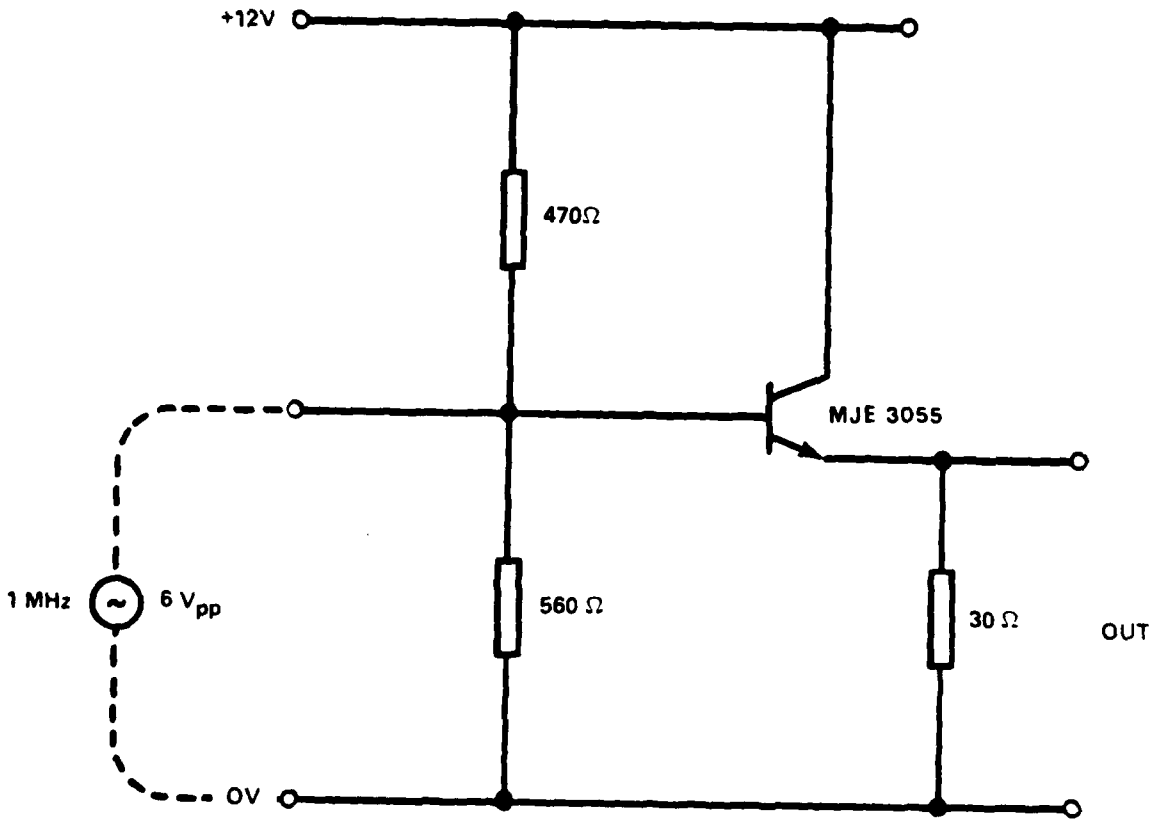


FIG 2

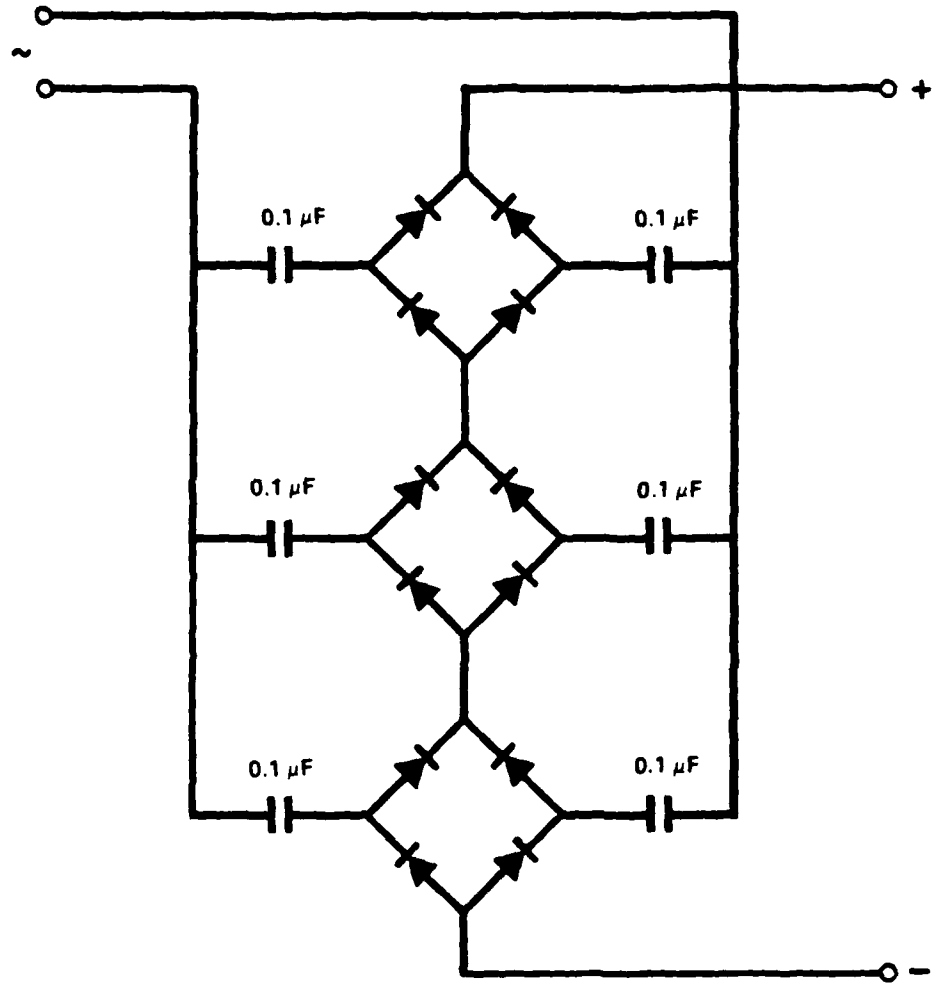

~
+
0.1 μF
0.1 μF
0.1 μF
0.1 μF
0.1 μF
0.1 μF
-

FIG 3

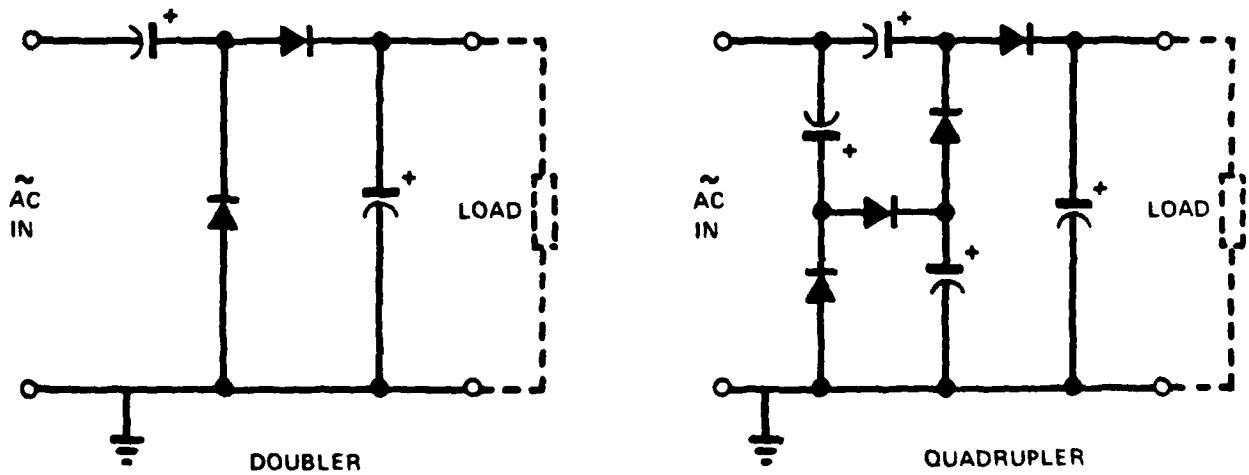

~
AC
IN
LOAD
DOUBLER
~
AC
IN
LOAD
QUADRUPLER

FIG 4

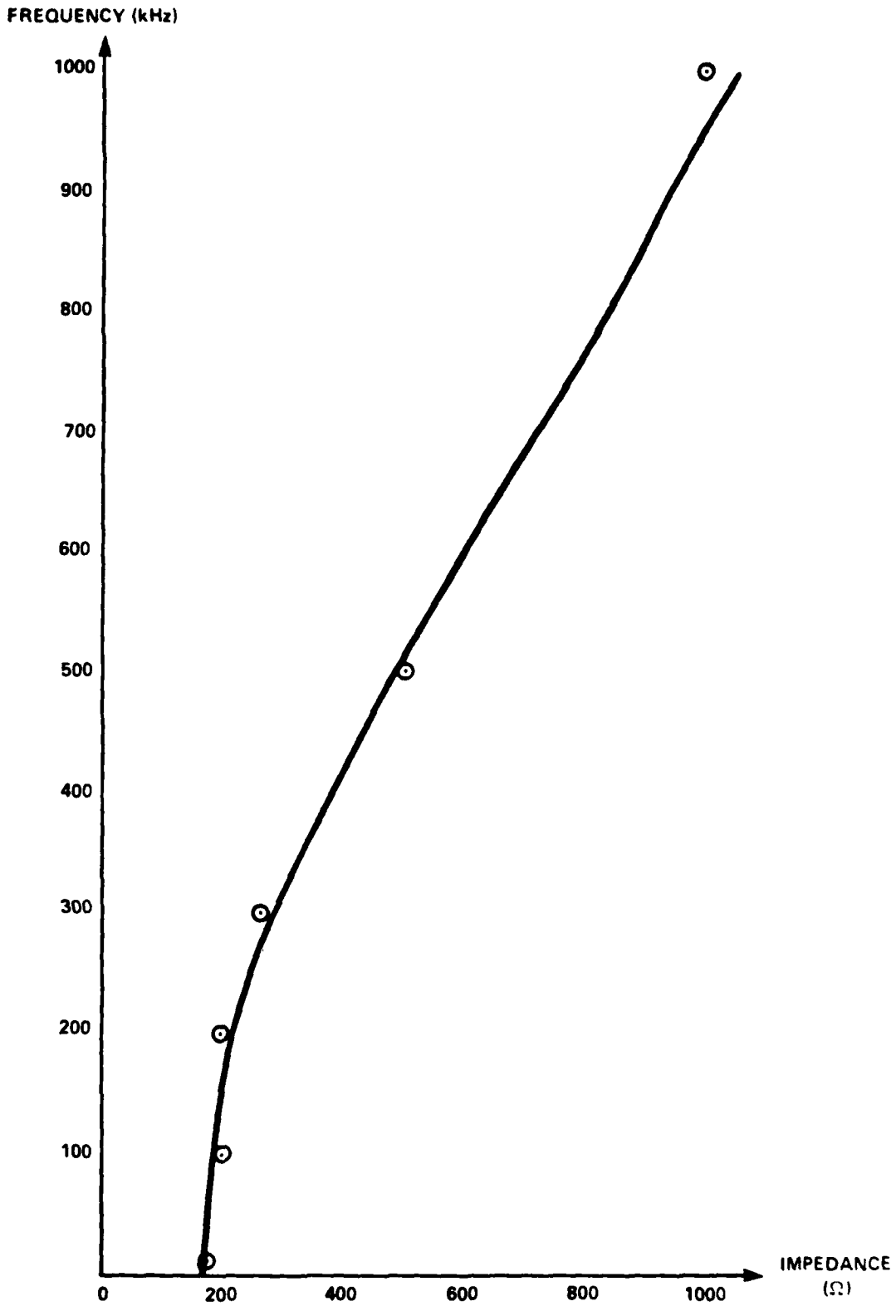
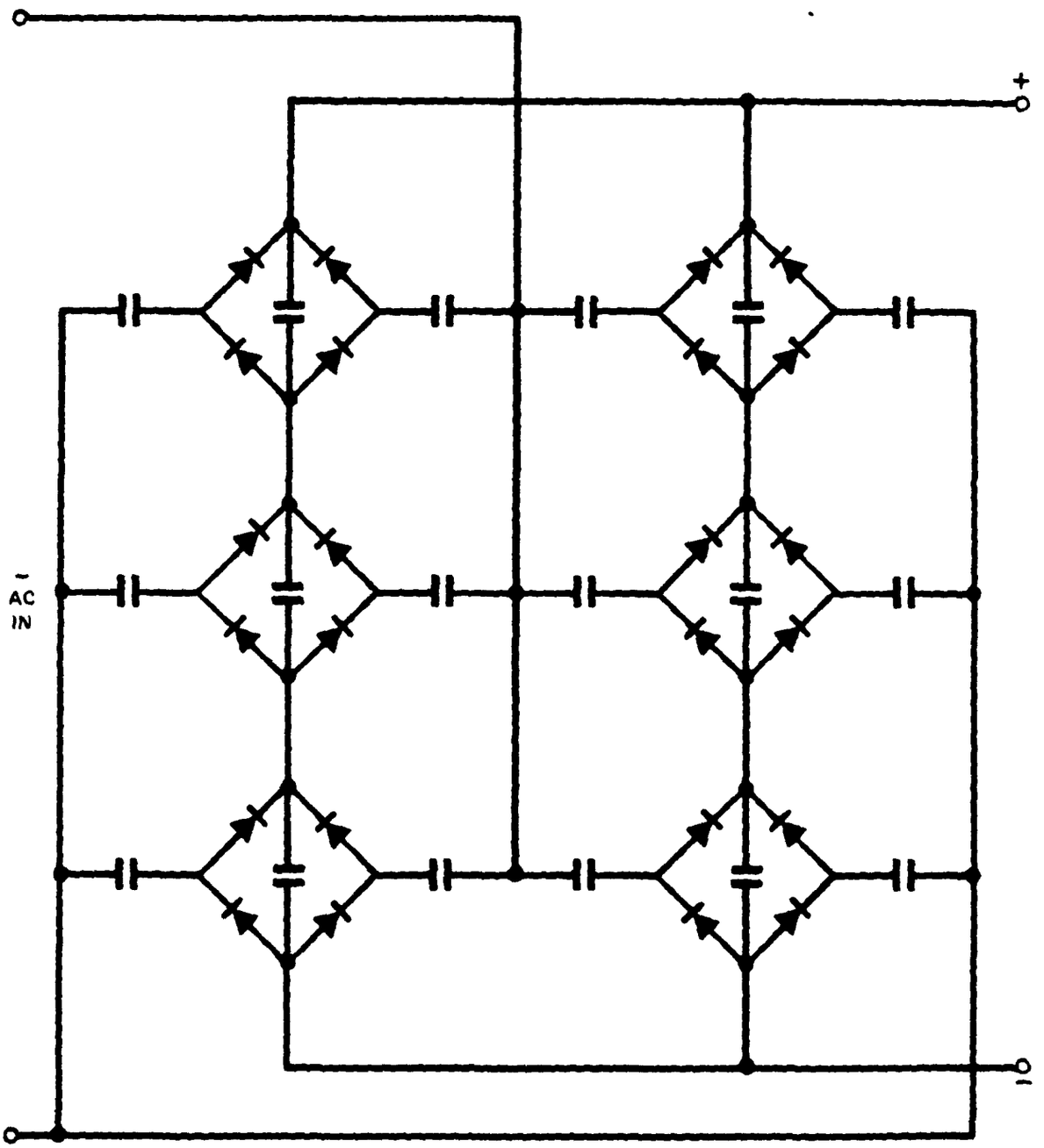
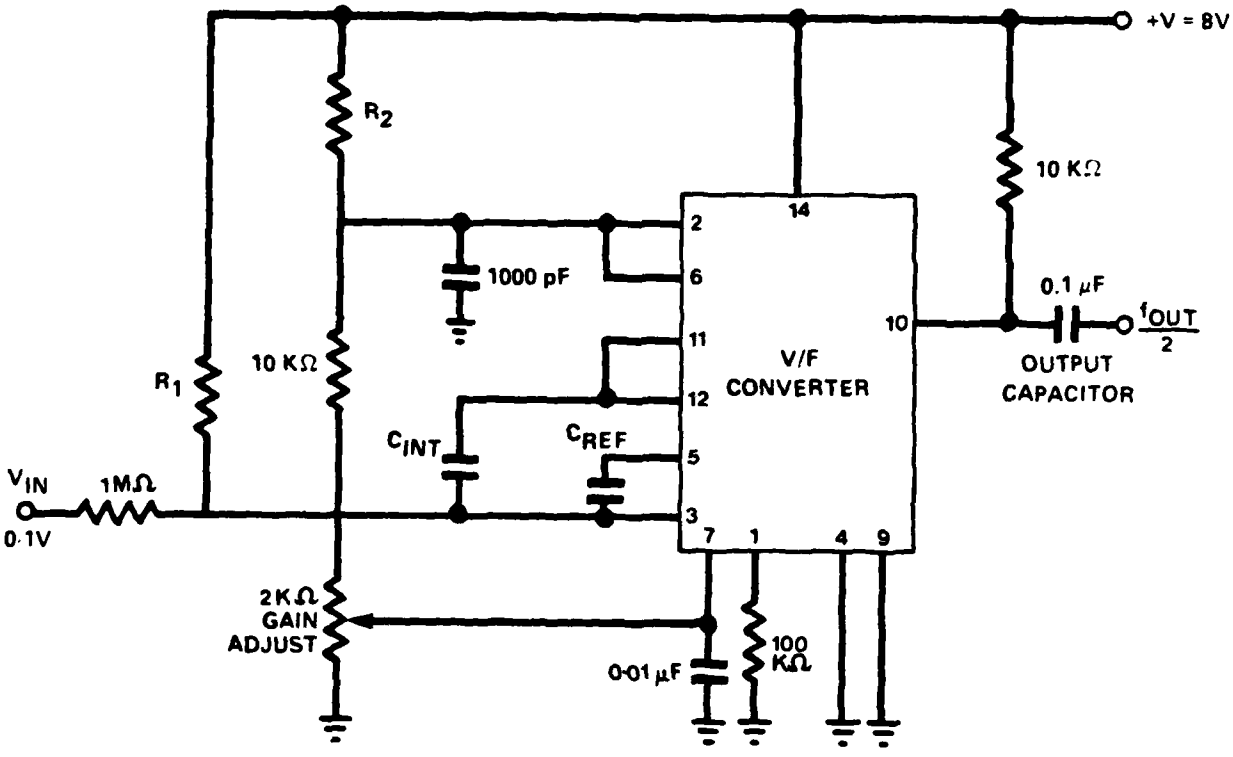

FREQUENCY (kHz)
1000
900
800
700
600
500
400
300
200
100
0
200
400
600
800
1000
IMPEDANCE
(Ω)

FIG 5



ALL CAPACITOR VALUES = 0.1 μF

FIG 6



R_1 = 820 KΩ R_2 = 7.5 KΩ + 5 KΩ VARIABLE RESISTOR

C_{INT} = 82 pF C_{REF} = 22 pF

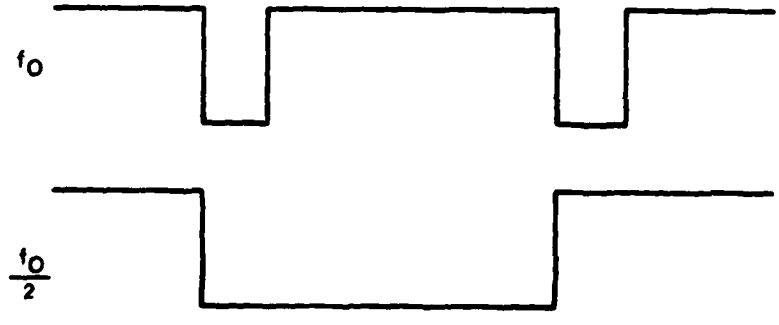


FIG 7

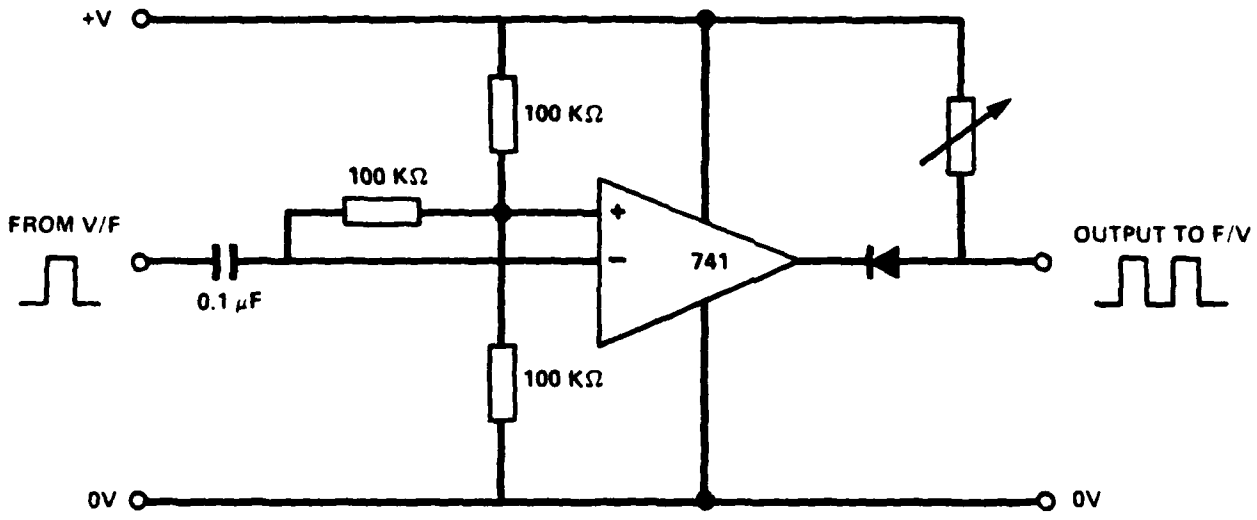

+V
100 KΩ
100 KΩ
FROM V/F
0.1 μF
741
OUTPUT TO F/V
100 KΩ
0V
0V

FIG 8

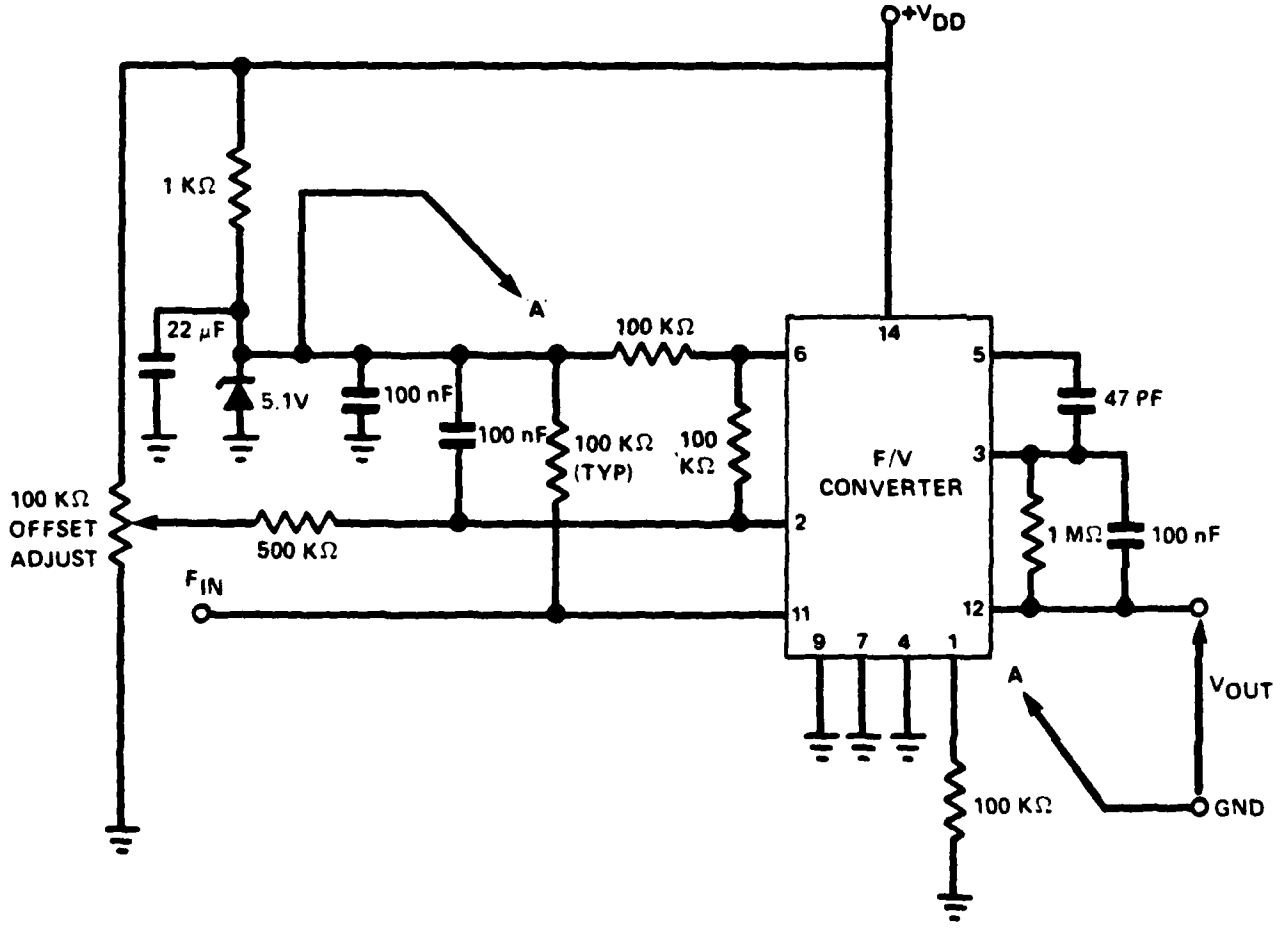

+VDD
1 KΩ
A
22 μF
100 KΩ
14
6
5
5.1V
100 nF
100 nF
100 KΩ (TYP)
100 KΩ
47 PF
F/V CONVERTER
3
100 KΩ OFFSET ADJUST
2
500 KΩ
1 MΩ
100 nF
FIN
11
12
9 7 4 1
A
VOUT
100 KΩ
GND

FIG 9

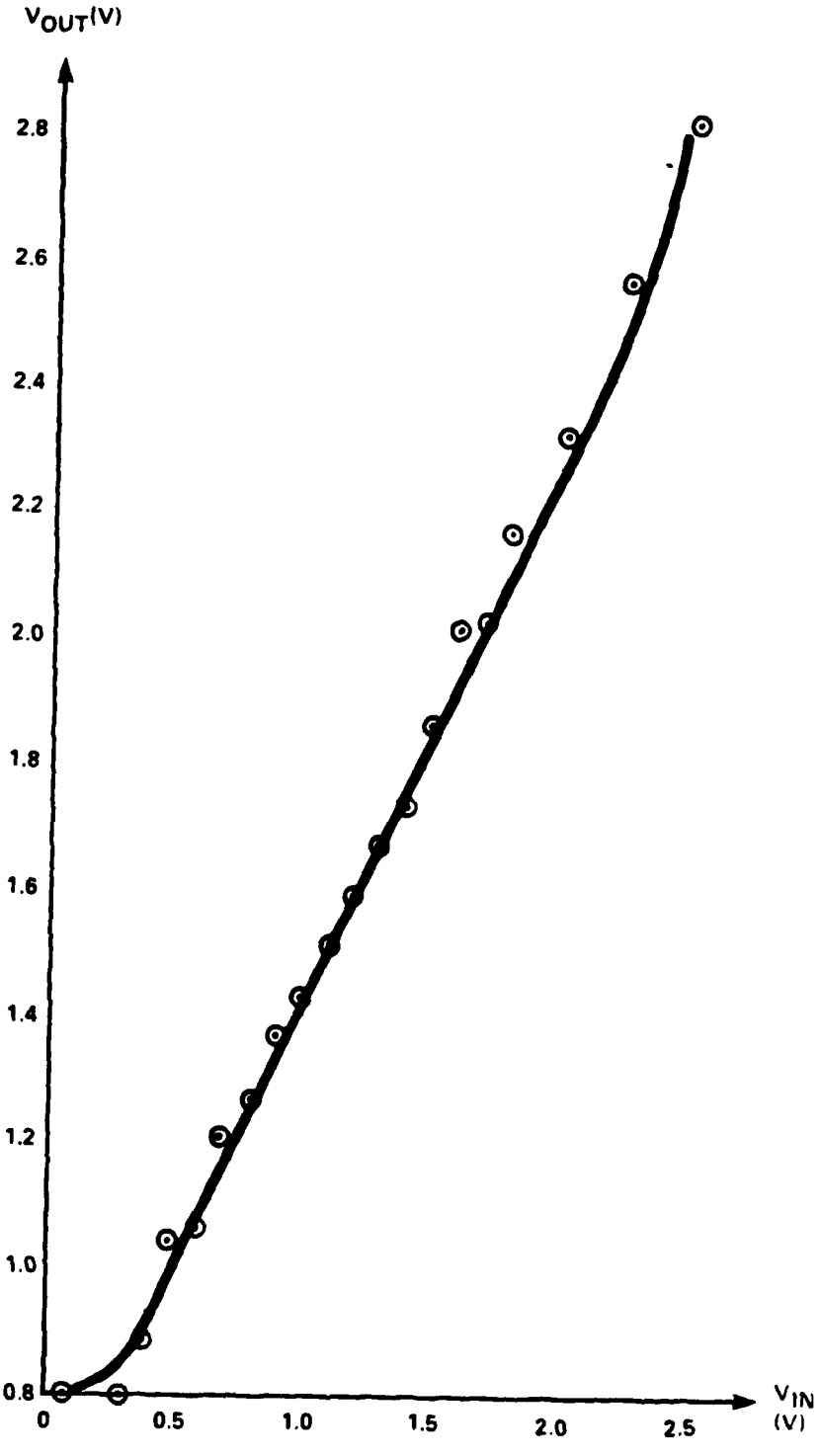


FIG 10

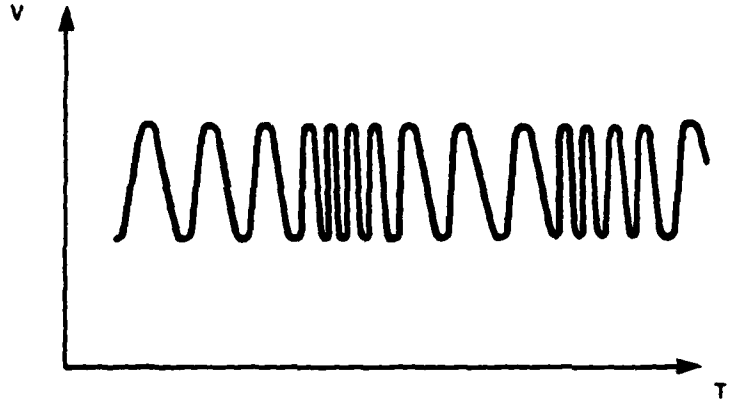


FIG 11.1 FREQUENCY MODULATION

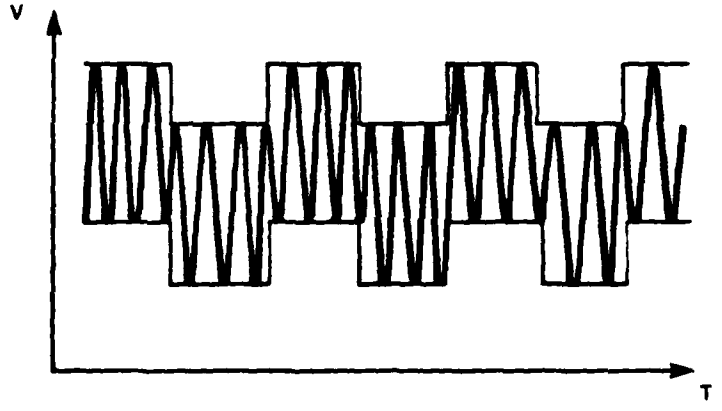


FIG 11.2 ADDING

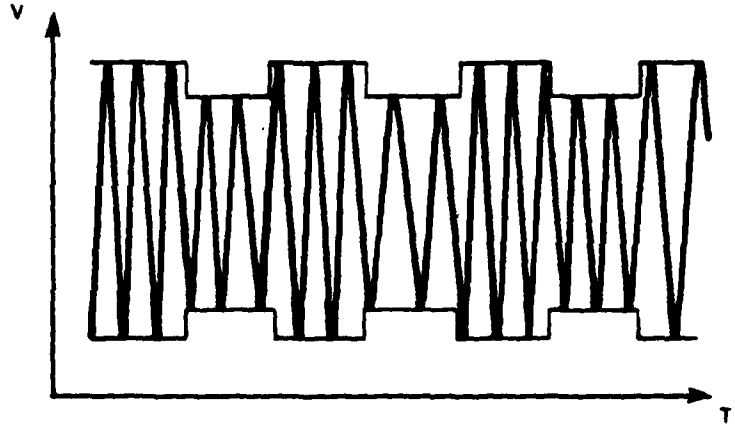


FIG 11.3 AMPLITUDE MODULATION

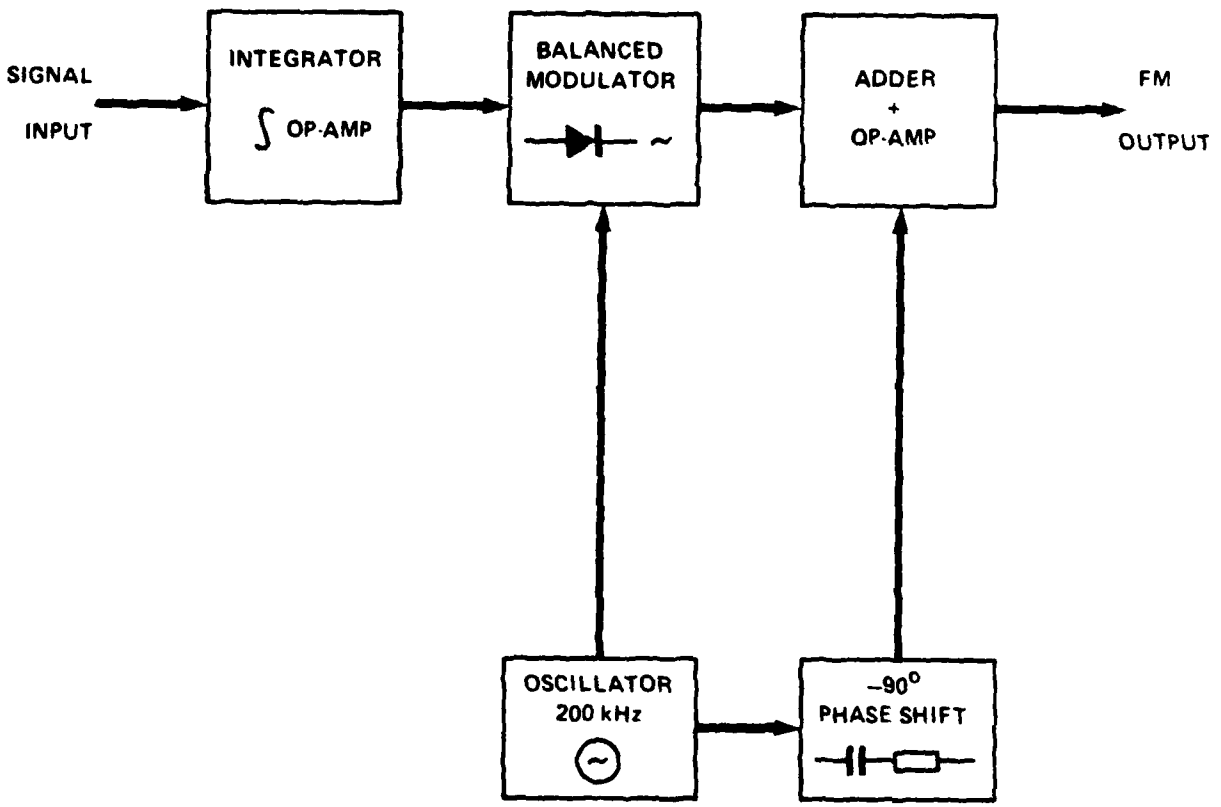
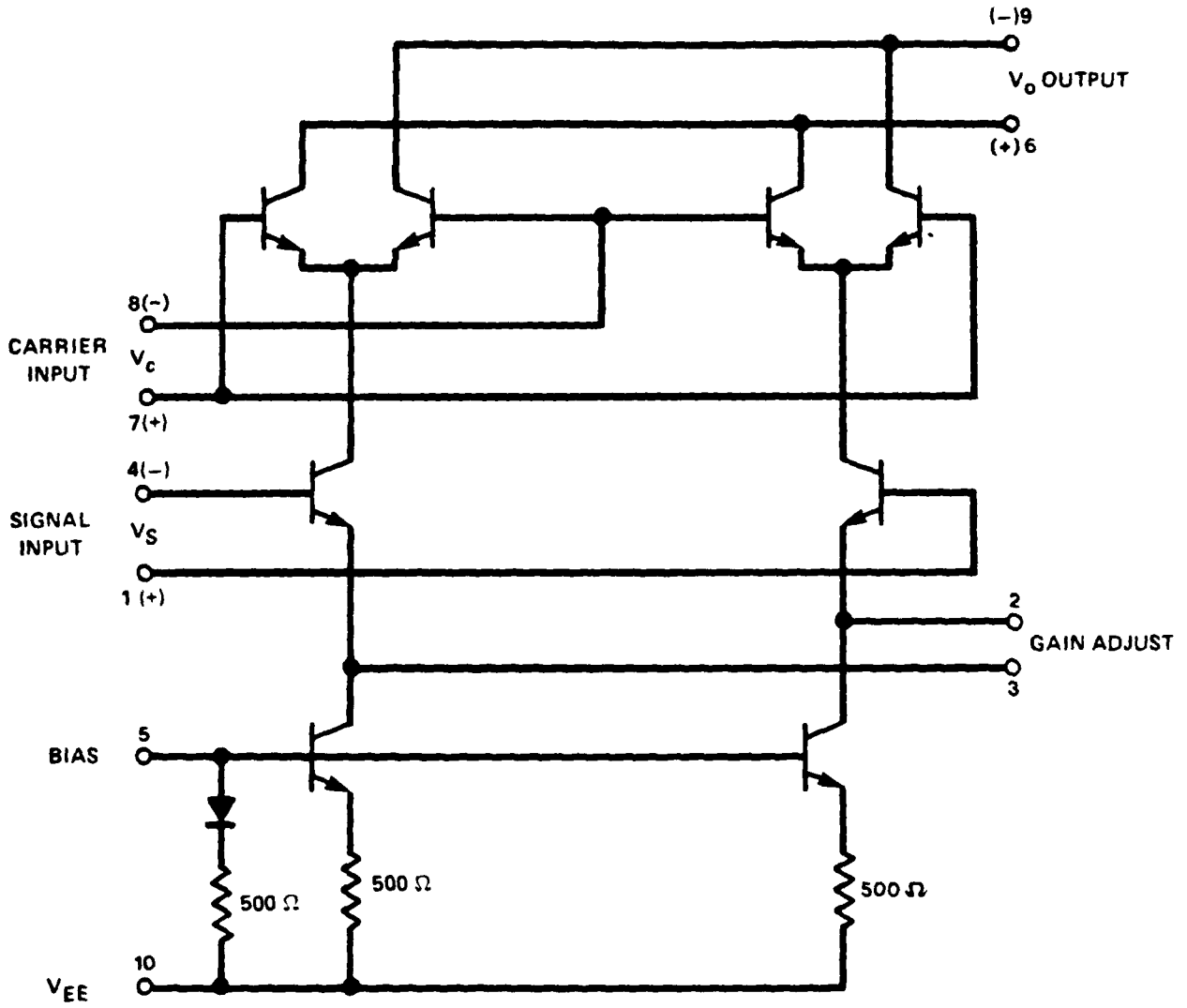

SIGNAL
INPUT
INTEGRATOR
∫ OP-AMP
BALANCED
MODULATOR
~
ADDER
+
OP-AMP
FM
OUTPUT
OSCILLATOR
200 kHz
~
-90°
PHASE SHIFT

FIG 12



(TOP VIEW)

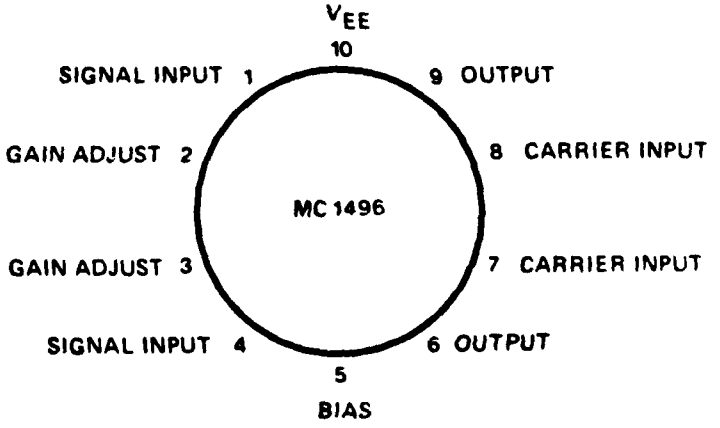


FIG 13

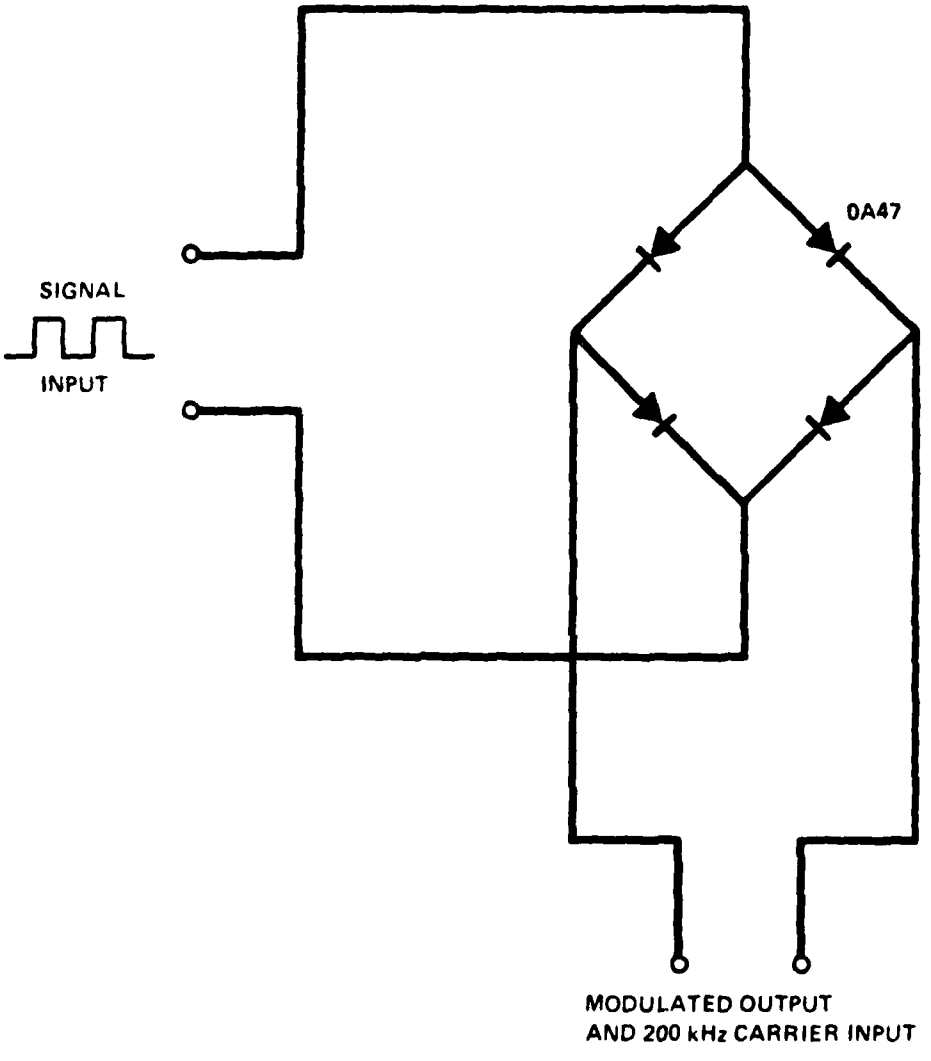

0A47
SIGNAL
INPUT
MODULATED OUTPUT
AND 200 kHz CARRIER INPUT

FIG 14

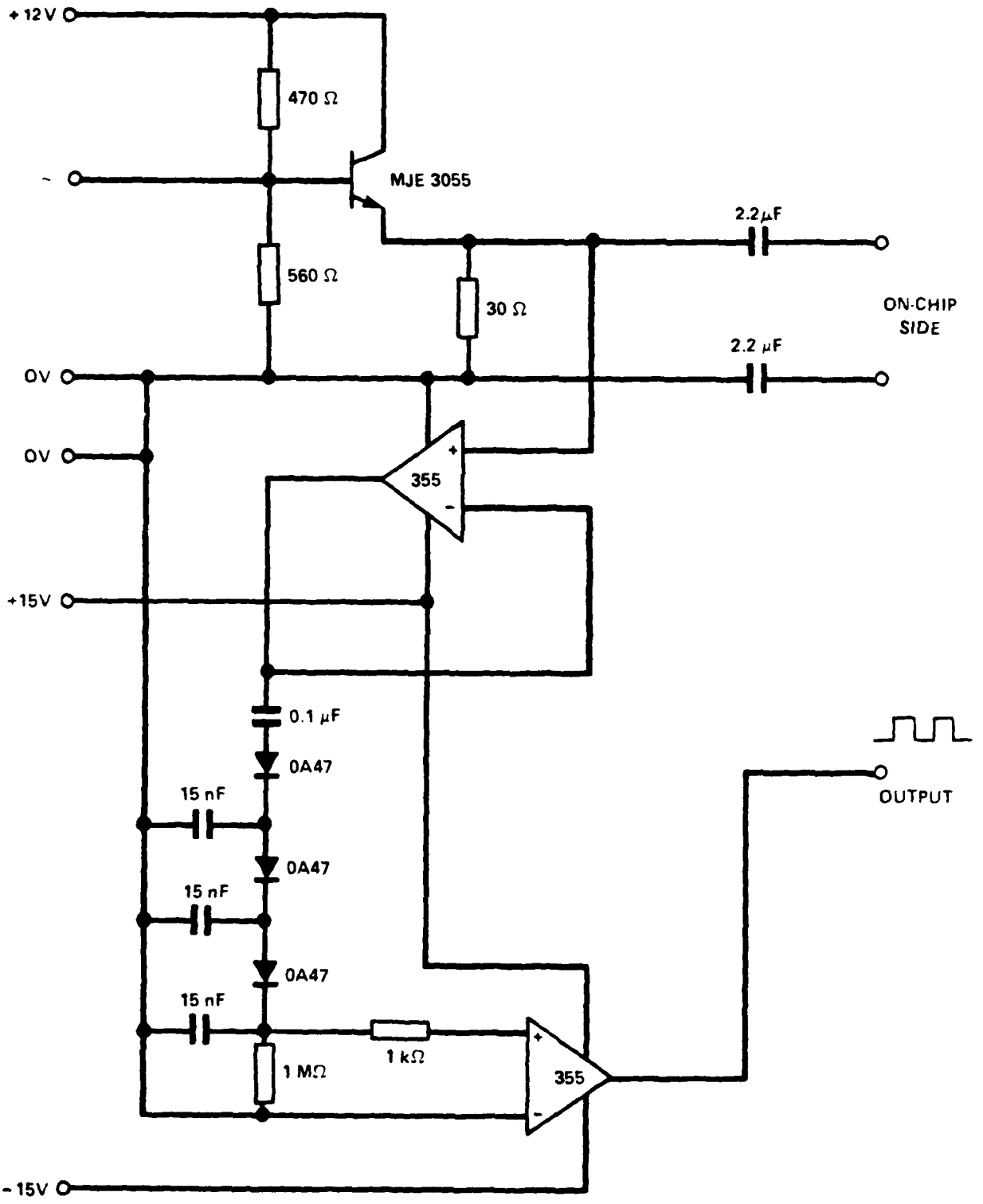

+12V
470 Ω
MJE 3055
2.2μF
560 Ω
30 Ω
ON-CHIP
SIDE
2.2 μF
0V
0V
355
+15V
0.1 μF
0A47
15 nF
0A47
15 nF
0A47
15 nF
1 kΩ
1 MΩ
355
OUTPUT
-15V

FIG 15

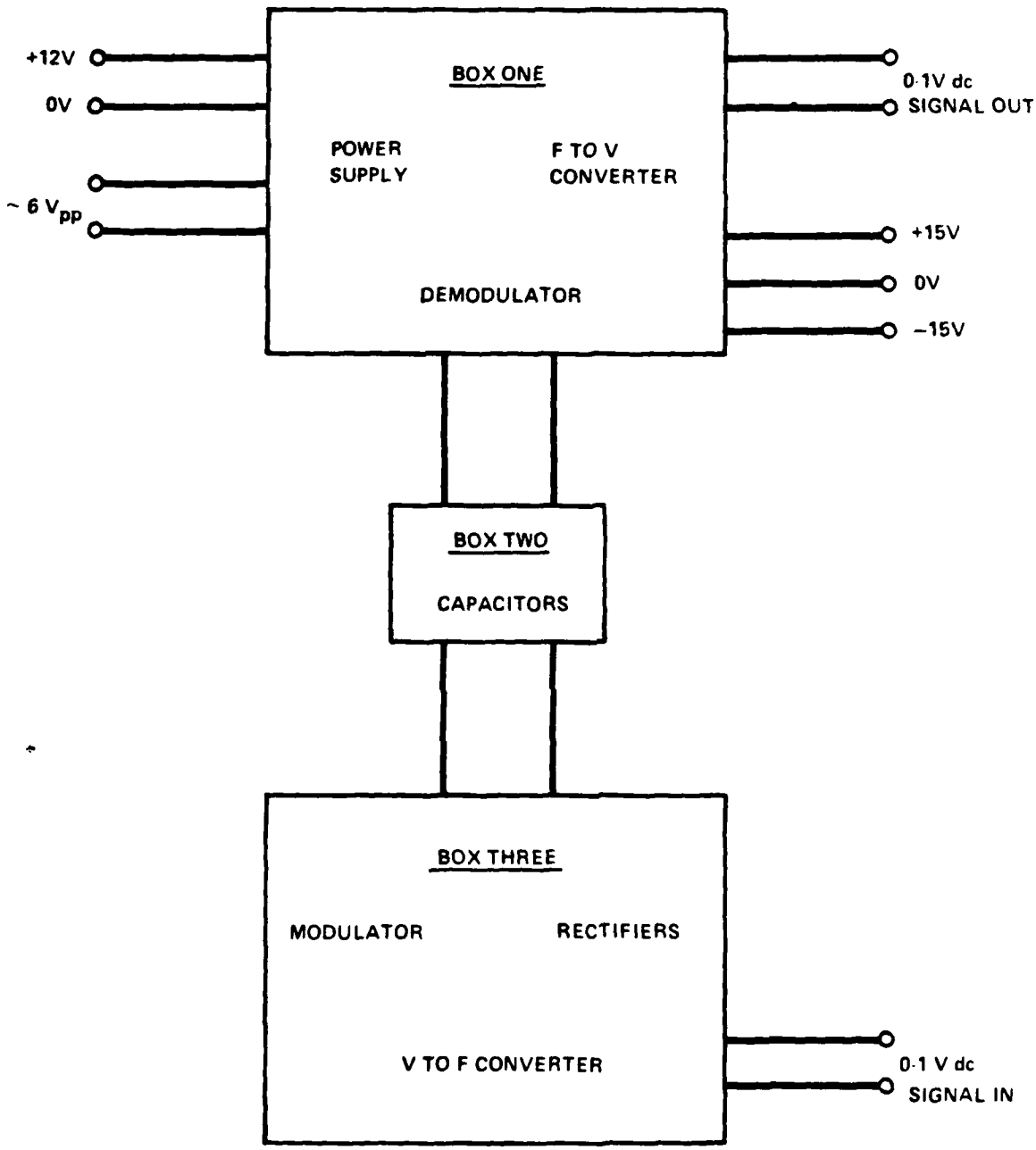

+12V
0V
~ 6 V_{pp}
BOX ONE
POWER SUPPLY
F TO V CONVERTER
DEMODULATOR
0·1V dc SIGNAL OUT
+15V
0V
−15V
BOX TWO
CAPACITORS
BOX THREE
MODULATOR
RECTIFIERS
V TO F CONVERTER
0·1 V dc SIGNAL IN

FIG 16

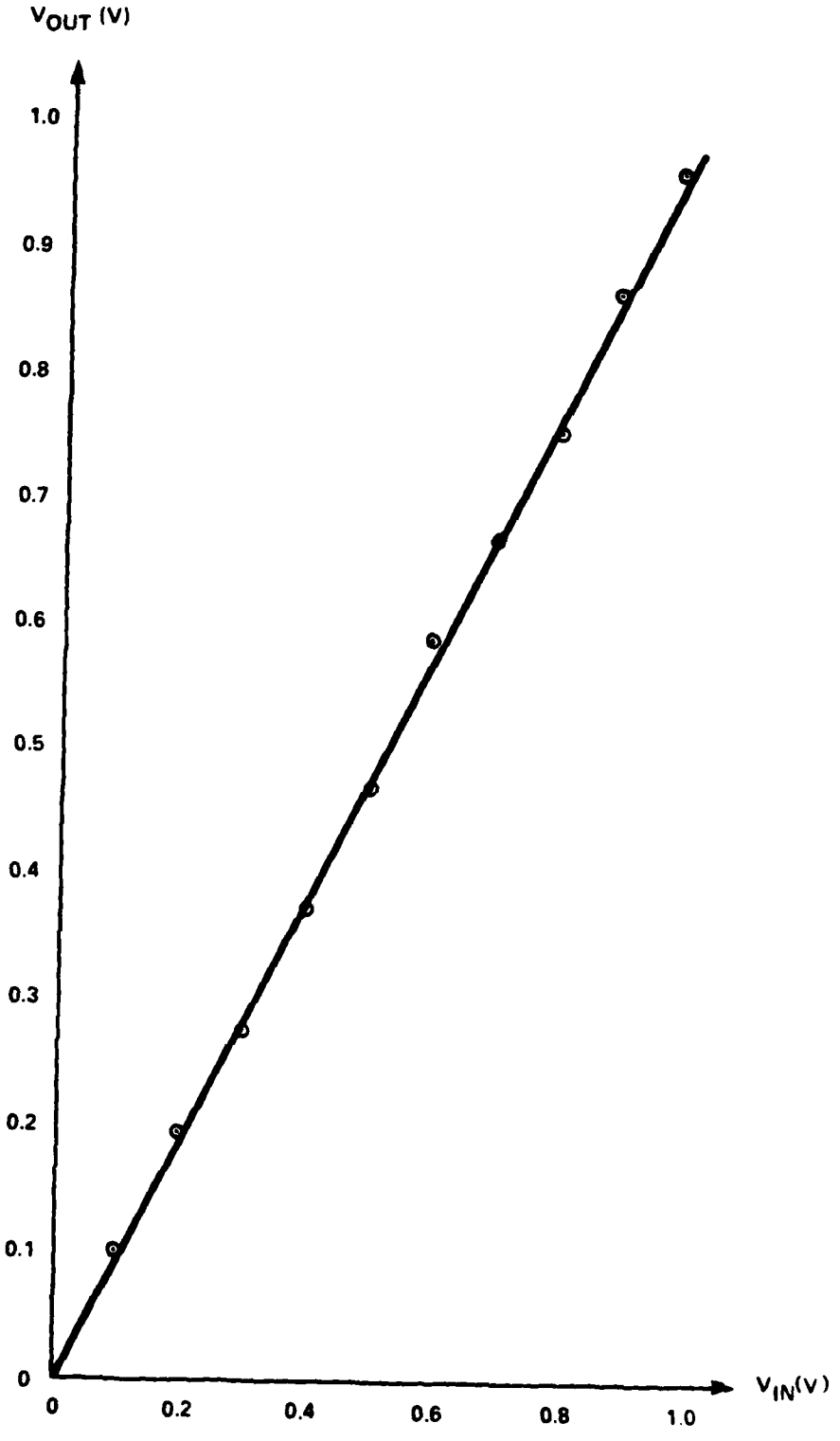


FIG 17

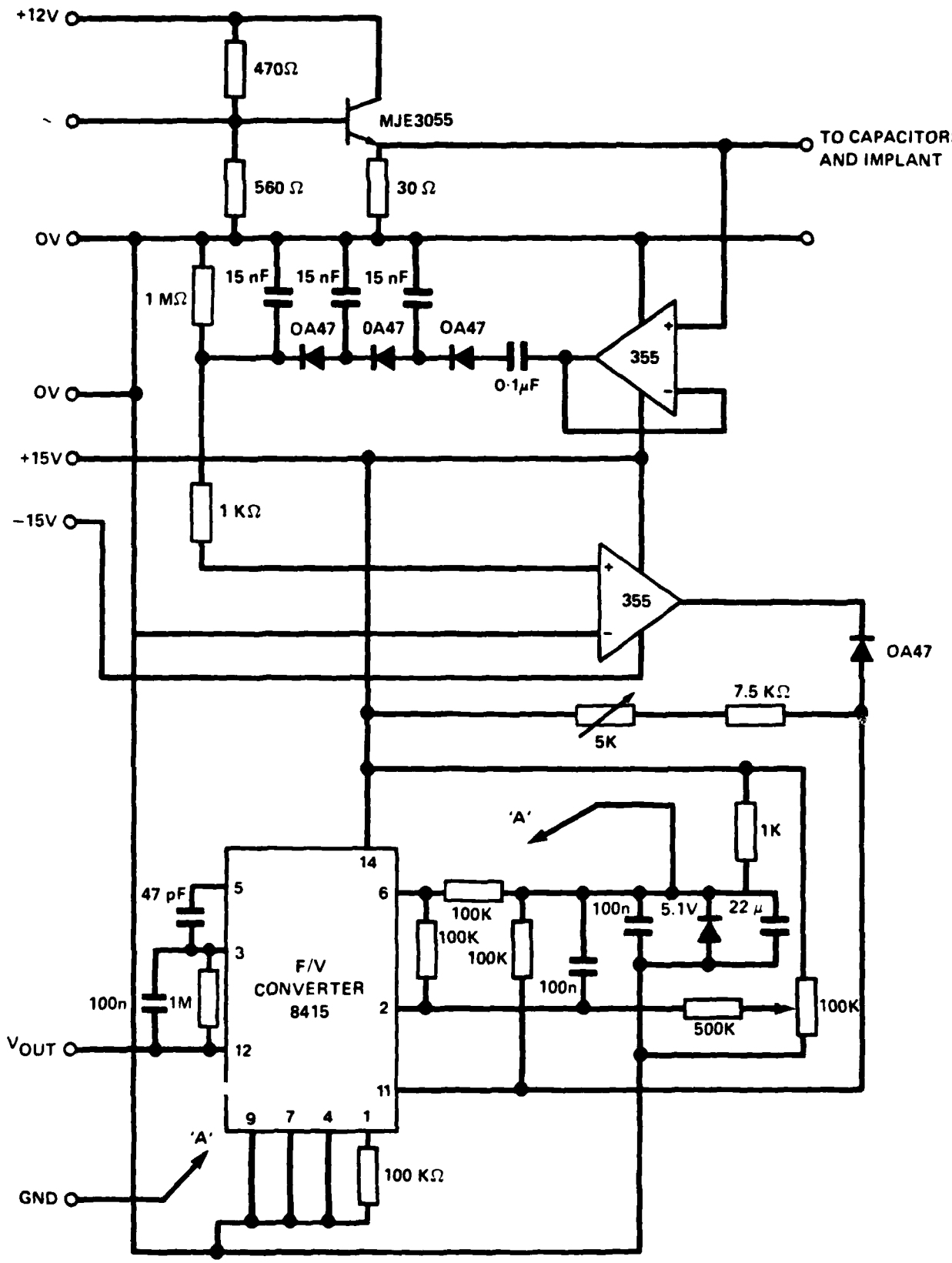

+12V
470Ω
MJE3055
TO CAPACITORS
AND IMPLANT
560 Ω
30 Ω
0V
1 MΩ
15 nF
15 nF
15 nF
OA47
OA47
OA47
0·1μF
355
0V
+15V
1 KΩ
−15V
355
OA47
7.5 KΩ
5K
'A'
1K
47 pF
14
5
6
100K
100K
100K
100n
5.1V
22 μ
3
F/V
CONVERTER
8415
100n
1M
2
100K
500K
VOUT
12
11
9
7
4
1
'A'
100 KΩ
GND

FIG 18

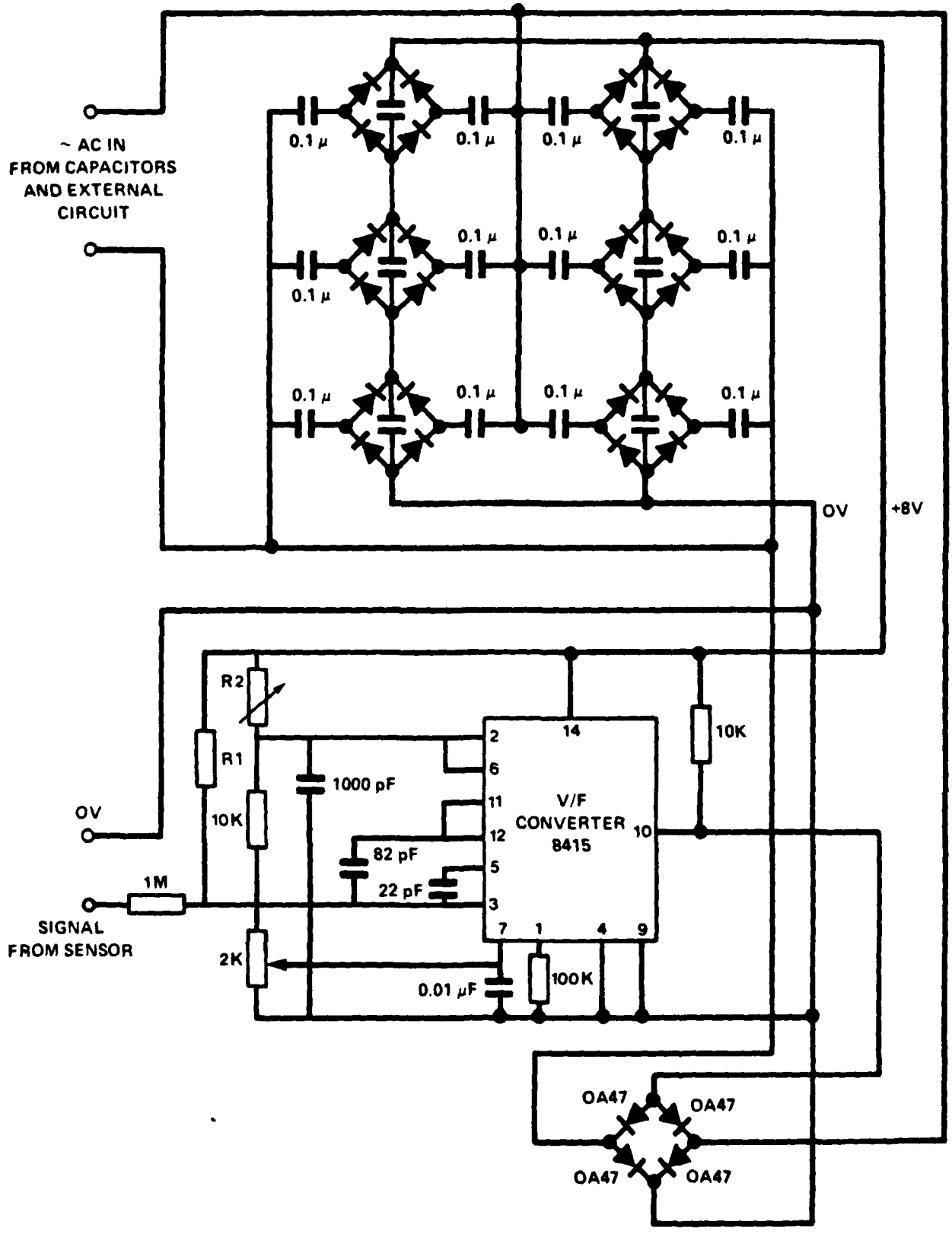

~ AC IN
FROM CAPACITORS
AND EXTERNAL
CIRCUIT
0.1 μ
OV
+8V
R2
R1
10K
1000 pF
82 pF
22 pF
1M
SIGNAL
FROM SENSOR
2K
0.01 μF
100K
V/F
CONVERTER
8415
14
2
6
11
12
5
3
7
1
4
9
10
OA47

FIG 19

END

FILMED

3-86

DTIC